32.1 A PVT-Tolerant Low-1/f Noise Dual-Loop Hybrid PLL in 0.18μm CMOS

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Implementing a low-jitter PLL with an integrated loop filter in a deep submicron CMOS process is a challenging task because of the relatively high 1/*f*-noise corner frequency, PVT variations, and leakage currents in capacitors. An all-digital PLL (ADPLL) [1, 2] overcomes PVT variations and reduces area by replacing area-consuming analog components in the PLL with digital components, such as a digitally controlled oscillator (DCO) and a digital loop filter (DLF). But it still has large jitter caused by flicker noise coming from the DCO, which is made of CMOS delay cells. One way to eliminate the 1/*f* noise and achieve low jitter is to set the bandwidth of the PLL high enough to sufficiently suppress the DCO noise. Unfortunately this method cannot be used for an application with a very low frequency reference clock because the bandwidth of the PLL should be lower than 1/10 of the frequency of the reference clock. A hybrid PLL improves the jitter performance by designing a dual-loop PLL, which has the required low bandwidth based on a digital PLL and has the ability to suppress the excessive 1/*f* noise with a high-bandwidth analog PLL.

Figure 32.1.1 shows the block diagram of the digital-analog hybrid PLL, which is mainly composed of a DCO and a digital PLL (DPLL). The DCO is implemented with a fractional-*N* PLL and the output frequency is controlled by the digital value *N*. Since the frequency of the DCO is controlled by the digital value, the frequency gain (*Kvco*) is fixed regardless of PVT variations. The internal VCO only covers a ±20% range (about 1.0 to 1.5GHz), while the following divider (div1) changes its ratio to make the output frequency cover a much wider range (20× tuning range). Since the tuning range of the VCO in the analog PLL is kept narrow, the design of the analog PLL is very simple.

In the digital PLL loop, the time-to-digital converter (T2D) digitizes the time difference between the input clock and the feedback clock. The 10b output from T2D is fed into the digital loop filter. The DLF generates the numerical control voltage corresponding to the analog control voltage of the conventional analog PLL. When the frequency of the reference clock is very low (~ 100kHz), a digital loop filter can be more economically implemented than a conventional analog loop filter, which occupies too big area to be integrated and is often implemented with off-chip components. To obtain the fine resolution and low jitter given limited resolution for the digital control, a ΔΣ modulator is placed between the DLF and the DCO. Also 5 multi-phase clocks from the VCO are used for a fractional divider to achieve further jitter reduction [3].

The advantage of this hybrid PLL is that we can independently adjust the loop bandwidths of the analog and digital loops to get smaller jitter, especially when the frequency of the reference clock is very low (~ 100kHz). Since the bandwidth of the single-loop PLL should be lower than 1/10 of the reference-clock frequency, flicker noise from the VCO cannot be suppressed efficiently. In this design, we kept the bandwidth of the analog PLL high enough (> 1.5MHz) to get sufficient noise suppression and to keep the area of the analog loop filter small. At the same time, the bandwidth of the digital loop is kept low (< 10kHz) using a simple digital loop filter.

The T2D generates a digital code that is proportional to the time difference between the input and the feedback clock. For low jitter, the T2D should have fine resolution. Figure 32.1.2 shows the block diagram and timing diagram of the T2D. The T2D is composed of a PFD, a charge pump, a voltage comparator and a counter. The PFD generates a pulse whose width is proportional to the time difference between the two inputs. During this period t_1, the capacitor C is charged by the current I_1. When both signals are high, C is discharged by the current I_2, which is k times smaller than I_1. During the discharge phase, the counter counts up until V_x reaches the reference voltage V_c; the node V_x is reset to V_c before being charged up again. By changing the current ratio between I_1 and I_2, we can control the discharging time and adjust the gain of the T2D. Since the VCO clock has a much higher frequency than the input clock, the T2D achieves fine resolution.

Figure 32.1.3 is the block diagram of the digital loop filter, which is a digital implementation of the conventional analog loop filter. Since the bandwidth of the loop is very low, aquiring the frequency and phase takes a long time. In order to speed up the locking behavior, frequency- and phase-acquisition aids are implemented. The frequency-acquisition aid sets up the initial value of the internal node and the phase-acquisition aid resets the output phase of the clock divider to align the phase to the input clock.

Figure 32.1.4(a) shows the phase noise measurement of the open-loop DCO and Fig. 32.1.4(b) shows the phase noise of the hybrid PLL. Since the bandwidth of the analog PLL used for the DCO is high (> 1.5MHz), we can observe that the VCO noise is suppressed up to this bandwidth. The phase noise at 100kHz offset is -123.5dBc/Hz and the phase noise curve below 100kHz comes mainly from the crystal oscillator. Using this DCO, the phase noise of the hybrid PLL also shows a similar curve except for the ΔΣ quantization noise around several MHz. The phase noise at 100kHz offset is -122.6dBc/Hz.

Figure 32.1.5 is the clock jitter histogram at 30.72MHz using a 30kHz reference clock. The long-term jitter, which was measured relative to the reference clock, is $150ps_{pp}$ which is only 0.46% of the period. Figure 32.1.6 shows how the jitter changes with the output frequency. The peak-to-peak jitter is relatively constant over frequency and, therefore, the jitter percentage slightly increases up to 2.8% of the period, which is smaller than previous works in the similar output frequency range [1, 2]. The graph shows only 10 to 170MHz clock outputs, but the maximum frequency extends to 400MHz using different values of div1. Figure 32.1.7 is the micrograph of the test chip and the core area is $0.23mm^2$. The DLF and the ΔΣ modulator are implemented in an FPGA for flexibility, and the estimated area of these blocks synthesized with a 0.18μm standard-cell library is $0.20mm^2$. The prototype chip dissipates 50mW from a 1.8V supply, which does not include the power consumption of the FPGA.

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References:
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[2] L. Xiu, et al., "A Novel All-Digital PLL with Software Adaptive Filter," *IEEE J. Solid-State Circuits*, vol. 39, pp. 476-483, Mar., 2004.
[3] C.-H. Heng and B.-S. Song, "A 1.8-GHz CMOS Fractional-N Frequency Synthesizer with Randomized Multiphase VCO," *IEEE J. Solid-State Circuits*, vol. 38, pp. 848-854, June, 2003.

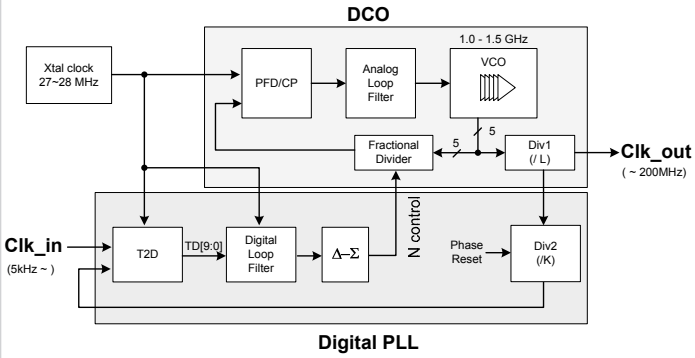


Figure 32.1.1: Dual-loop hybrid PLL block diagram.

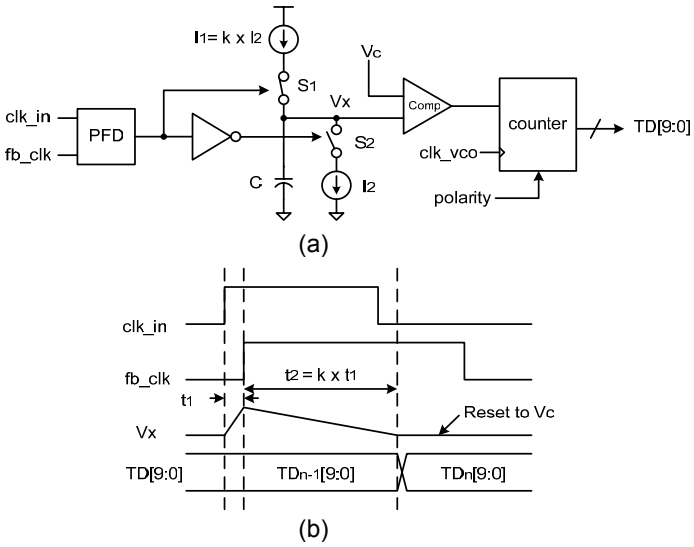
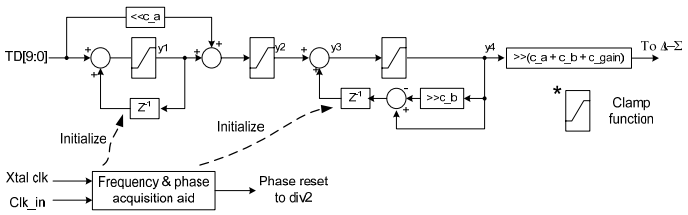


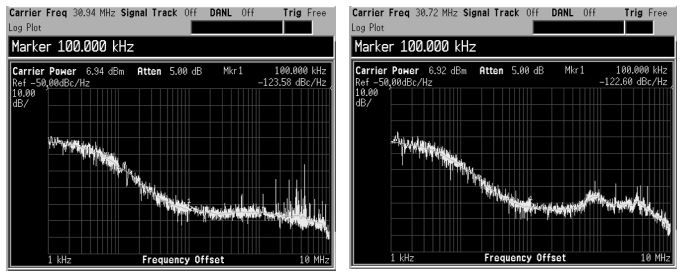
Figure 32.1.2: Time-to-digital converter (T2D) (a) block diagram (b) timing diagram.



$$H_{LF}(z) = K\left(1 + \frac{a}{1 - z^{-1}}\right) \cdot \frac{b}{1 - (1-b) \cdot z^{-1}}$$

$$where, a = 2^{-c\_a}, b = 2^{-c\_b}, K = 2^{-c\_gain}$$

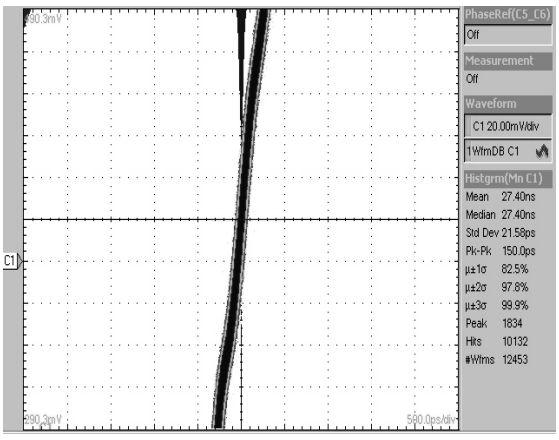
Figure 32.1.3: Digital loop filter.



Phase noise @100kHz offset = -123.5dBc/Hz (a)

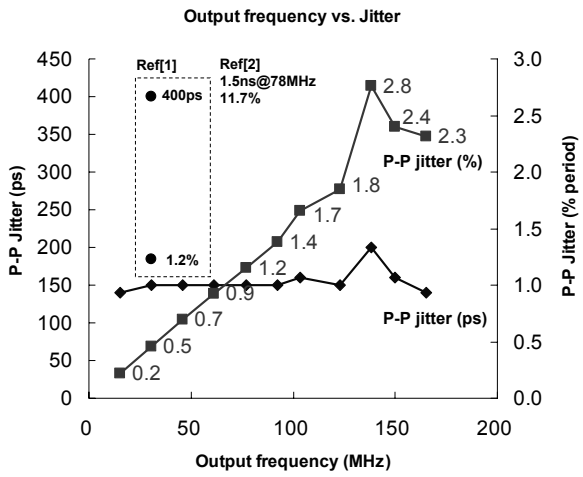
Phase noise @100kHz offset = -122.6dBc/Hz (b)

Figure 32.1.4: Phase noise: (a) Open-loop DCO (b) PLL locked to 30kHz.



30kHz x 1024 = 30.72MHz
Triggered at reference clock, P-P jitter = 150ps (0.46% clk period)

Figure 32.1.5: Output clock jitter histogram.



• Clock jitter is less than 2.8% of the clock period

Figure 32.1.6: Jitter versus output frequency.

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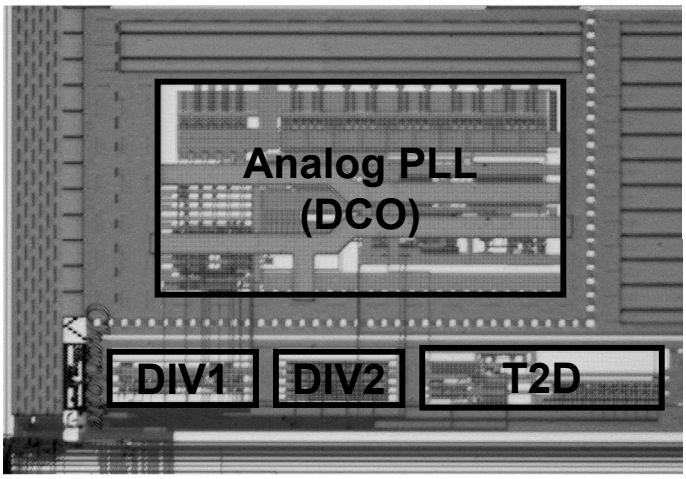

Figure 32.1.7: Chip micrograph.

